FIG. 1

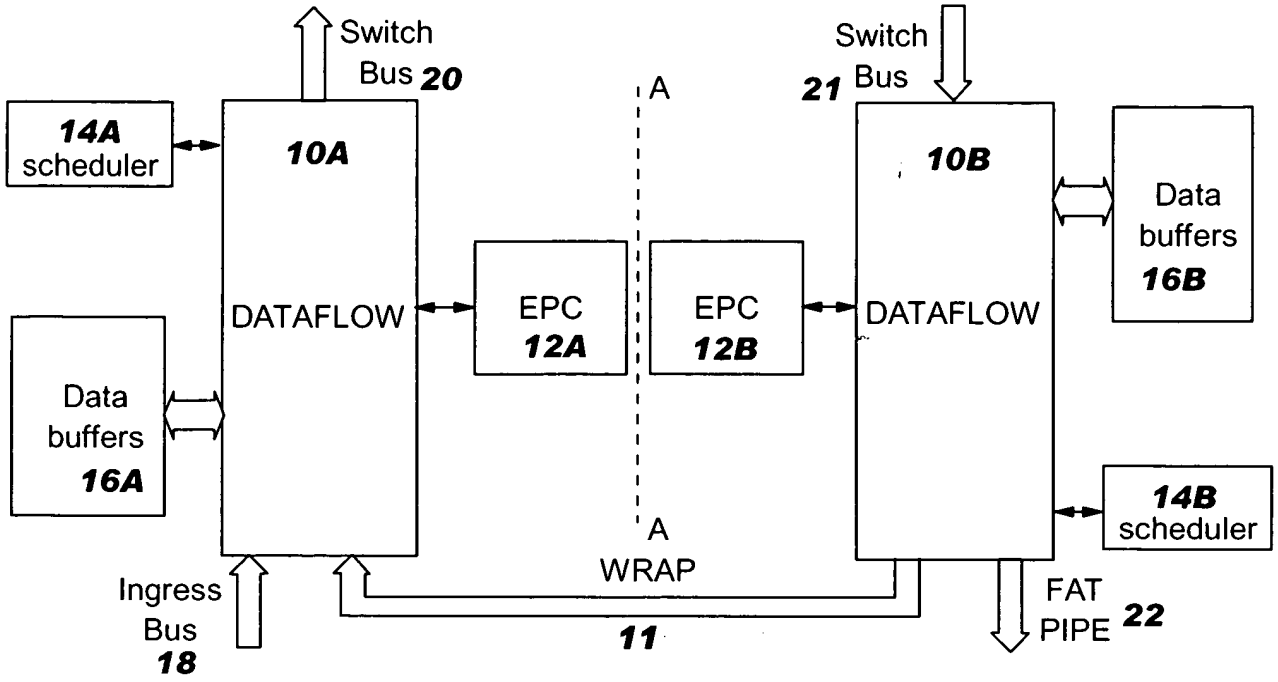

Switch Bus 20
Switch Bus 21
A
14A scheduler
10A
DATAFLOW
EPC 12A
EPC 12B
10B
DATAFLOW
Data buffers 16B
Data buffers 16A
14B scheduler
A
WRAP
Ingress Bus 18
11
FAT PIPE 22

FIG. 2

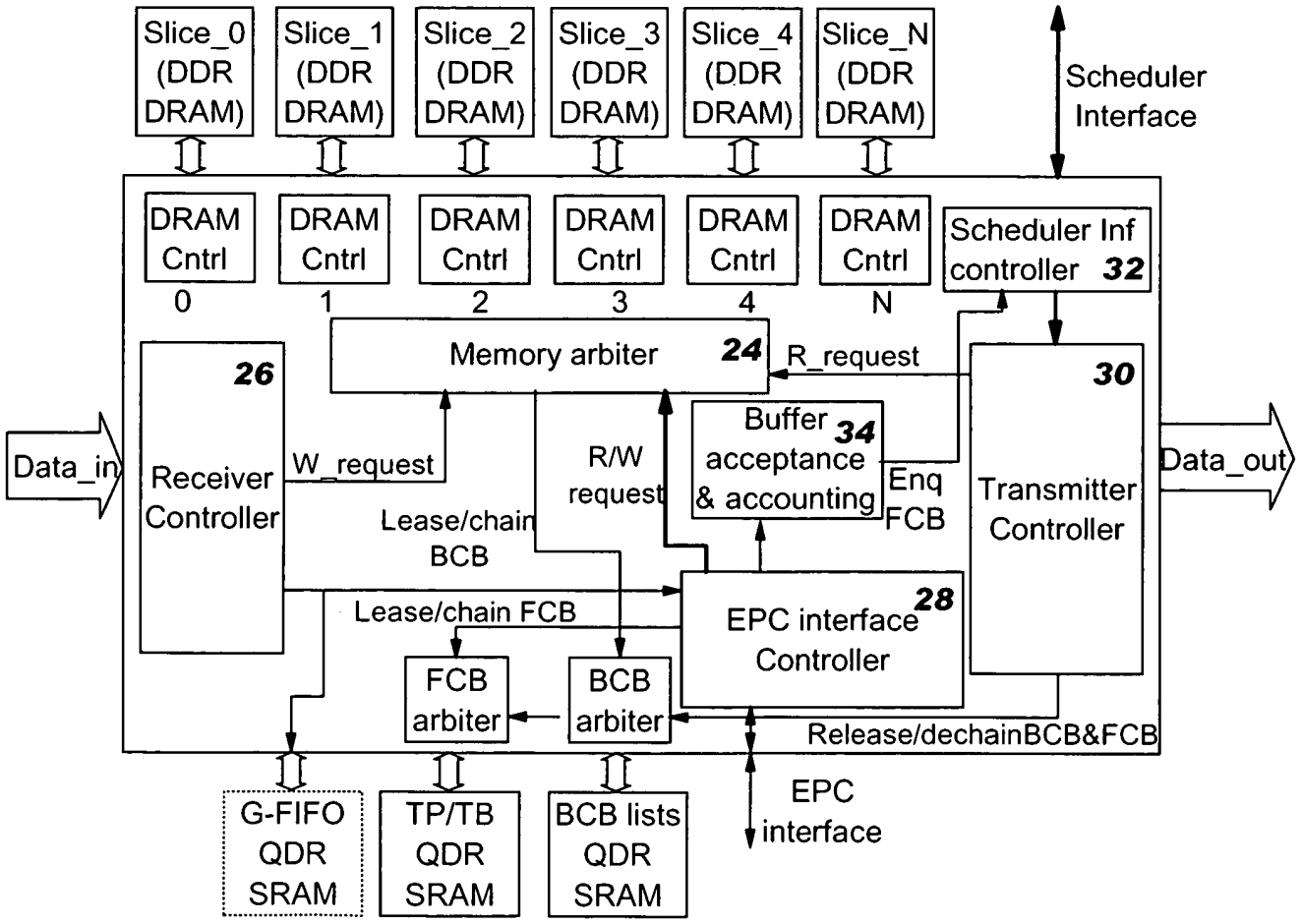

Slice_0 (DDR DRAM)
Slice_1 (DDR DRAM)
Slice_2 (DDR DRAM)
Slice_3 (DDR DRAM)
Slice_4 (DDR DRAM)
Slice_N (DDR DRAM)
Scheduler Interface
DRAM Cntrl 0
DRAM Cntrl 1
DRAM Cntrl 2
DRAM Cntrl 3
DRAM Cntrl 4
DRAM Cntrl N
Scheduler Inf controller 32
Memory arbiter 24
R_request
26
Receiver Controller
W_request
R/W request
Buffer acceptance & accounting 34
Enq FCB
30
Transmitter Controller
Data_in
Data_out
Lease/chain BCB
Lease/chain FCB
EPC interface Controller 28
FCB arbiter
BCB arbiter
Release/dechainBCB&FCB
G-FIFO QDR SRAM
TP/TB QDR SRAM
BCB lists QDR SRAM
EPC interface

FIG. 3

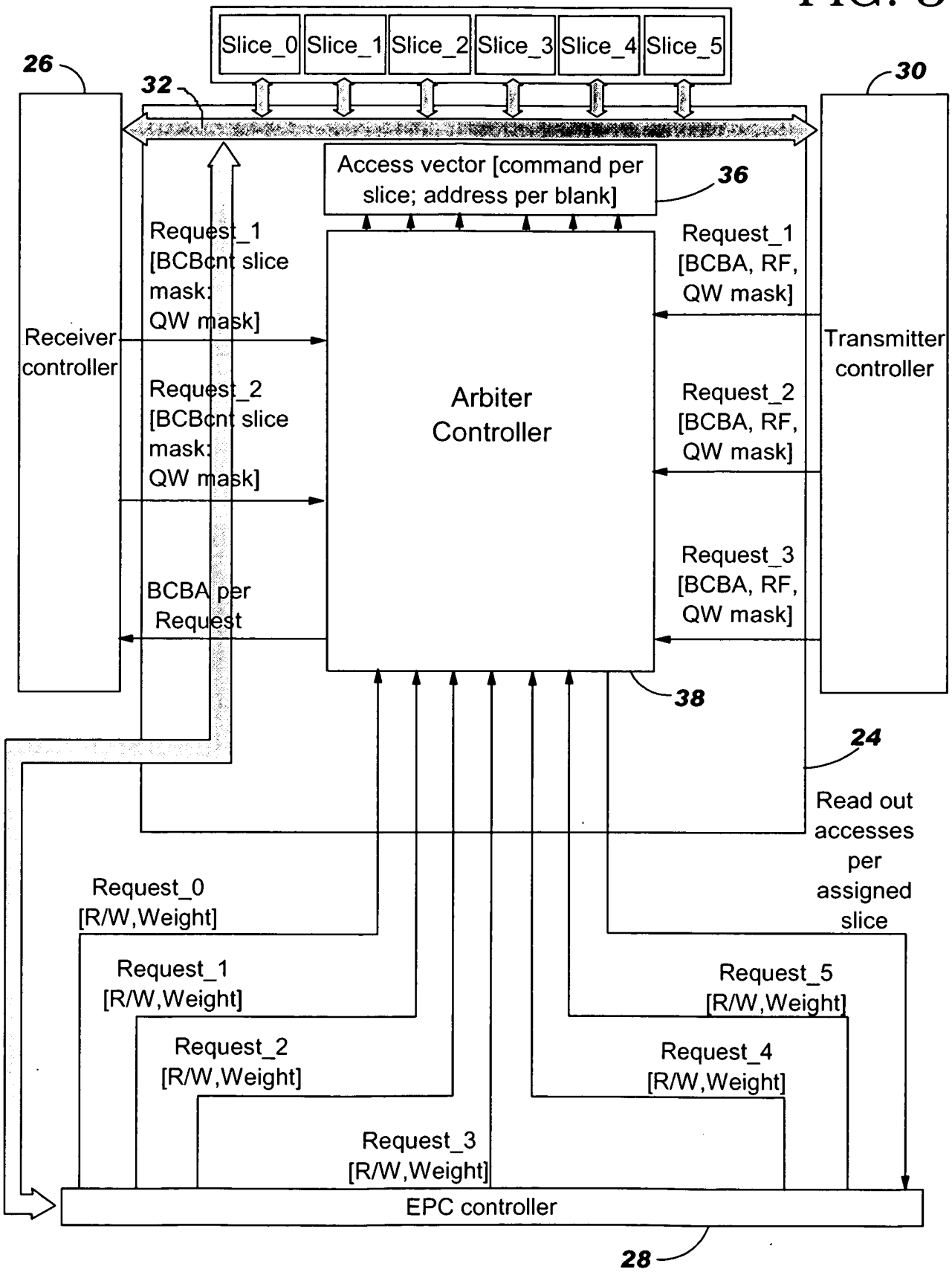

Slice_0
Slice_1
Slice_2
Slice_3
Slice_4
Slice_5
26
32
30
Access vector [command per slice; address per blank]
36
Request_1 [BCBcnt slice mask; QW mask]
Request_1 [BCBA, RF, QW mask]
Receiver controller
Transmitter controller
Request_2 [BCBcnt slice mask; QW mask]
Arbiter Controller
Request_2 [BCBA, RF, QW mask]
Request_3 [BCBA, RF, QW mask]
BCBA per Request
38
24
Read out accesses per assigned slice
Request_0 [R/W,Weight]
Request_1 [R/W,Weight]
Request_5 [R/W,Weight]
Request_2 [R/W,Weight]
Request_4 [R/W,Weight]
Request_3 [R/W,Weight]
EPC controller
28

FIG. 4

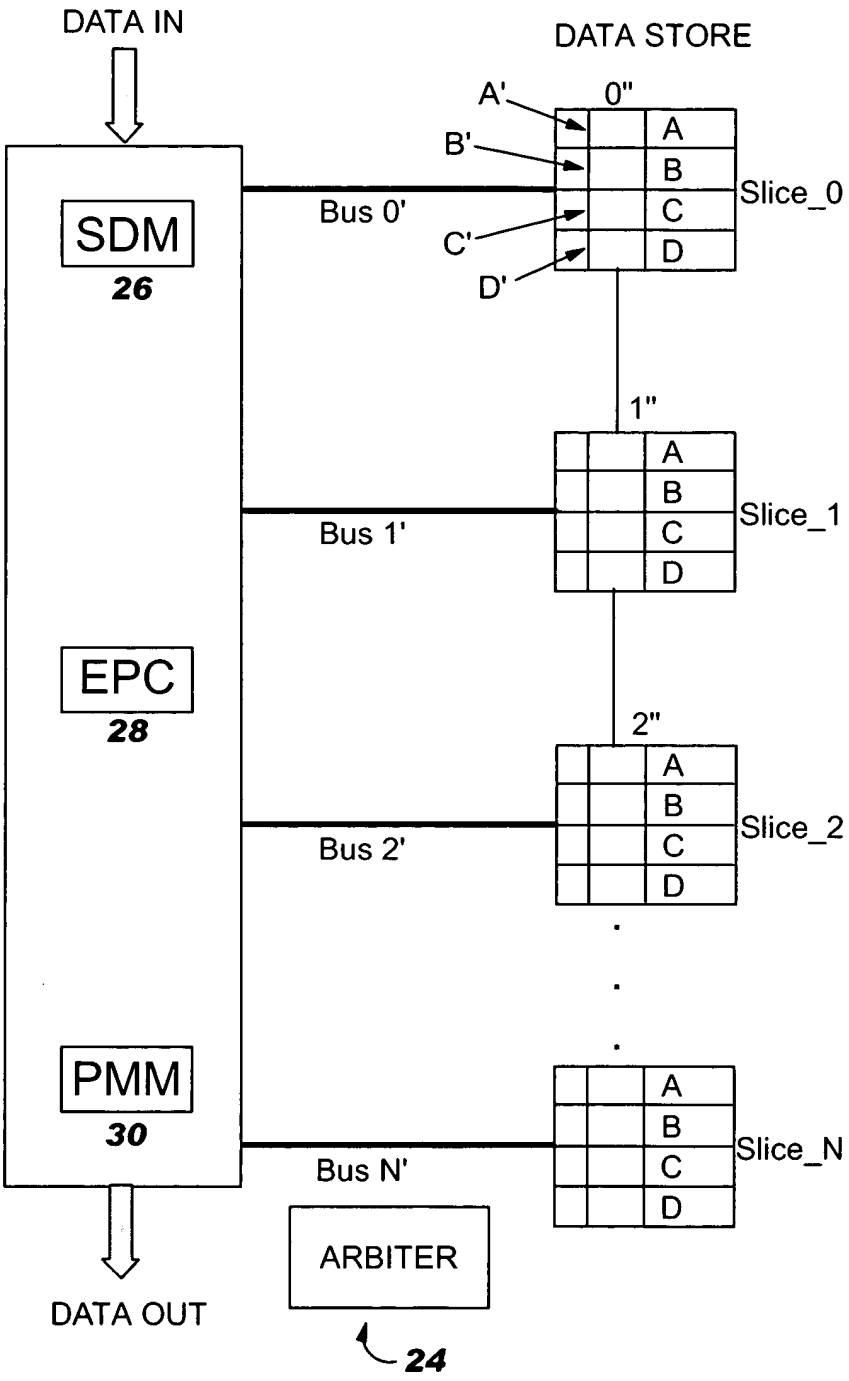

DATA IN
DATA STORE
A'
0"
B'
A
B
C
D
Slice_0
Bus 0'
C'
D'
SDM
26
1"
Slice_1
Bus 1'
EPC
28
2"
Slice_2
Bus 2'
PMM
30
Slice_N
Bus N'
ARBITER
DATA OUT
24

FIG. 5

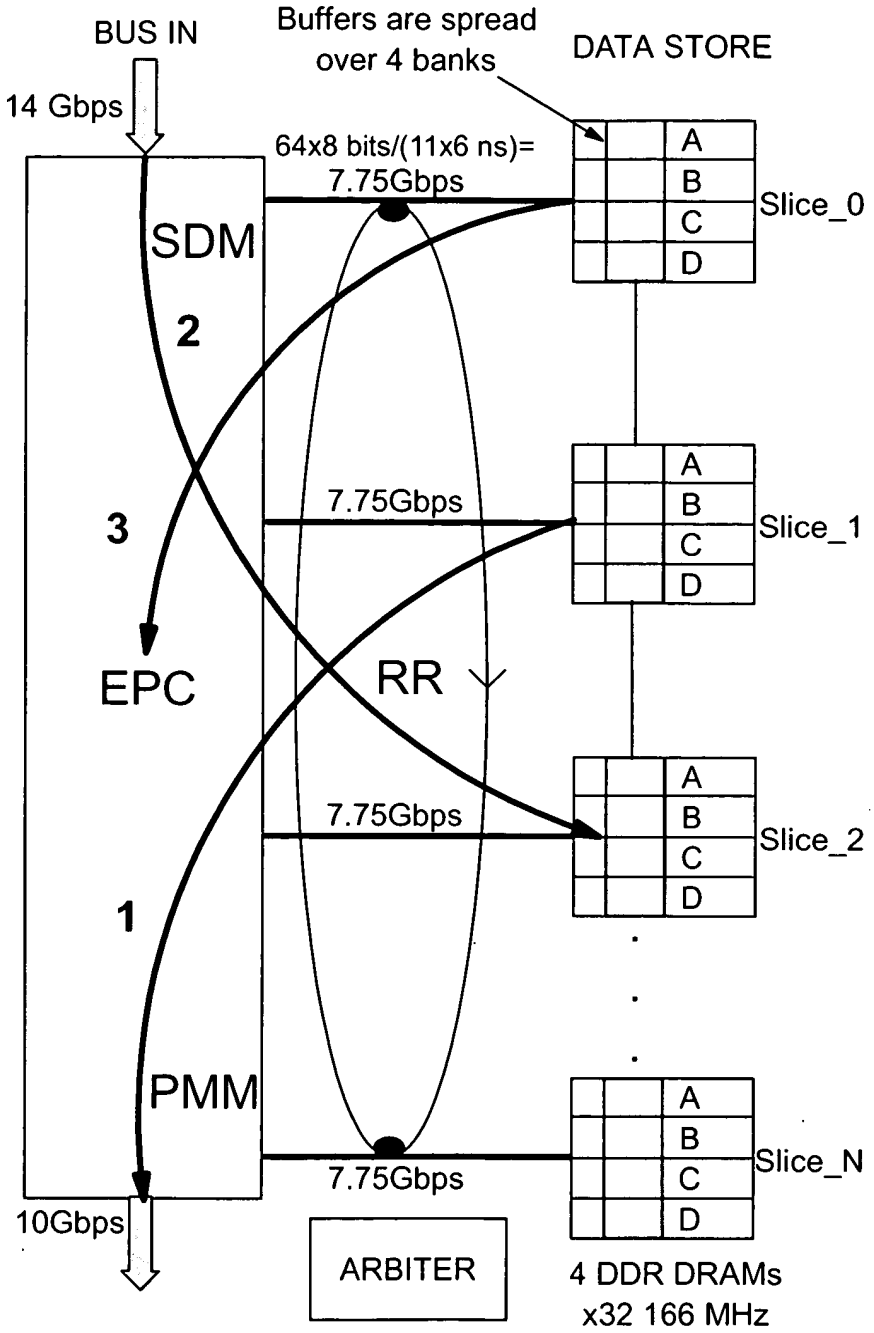
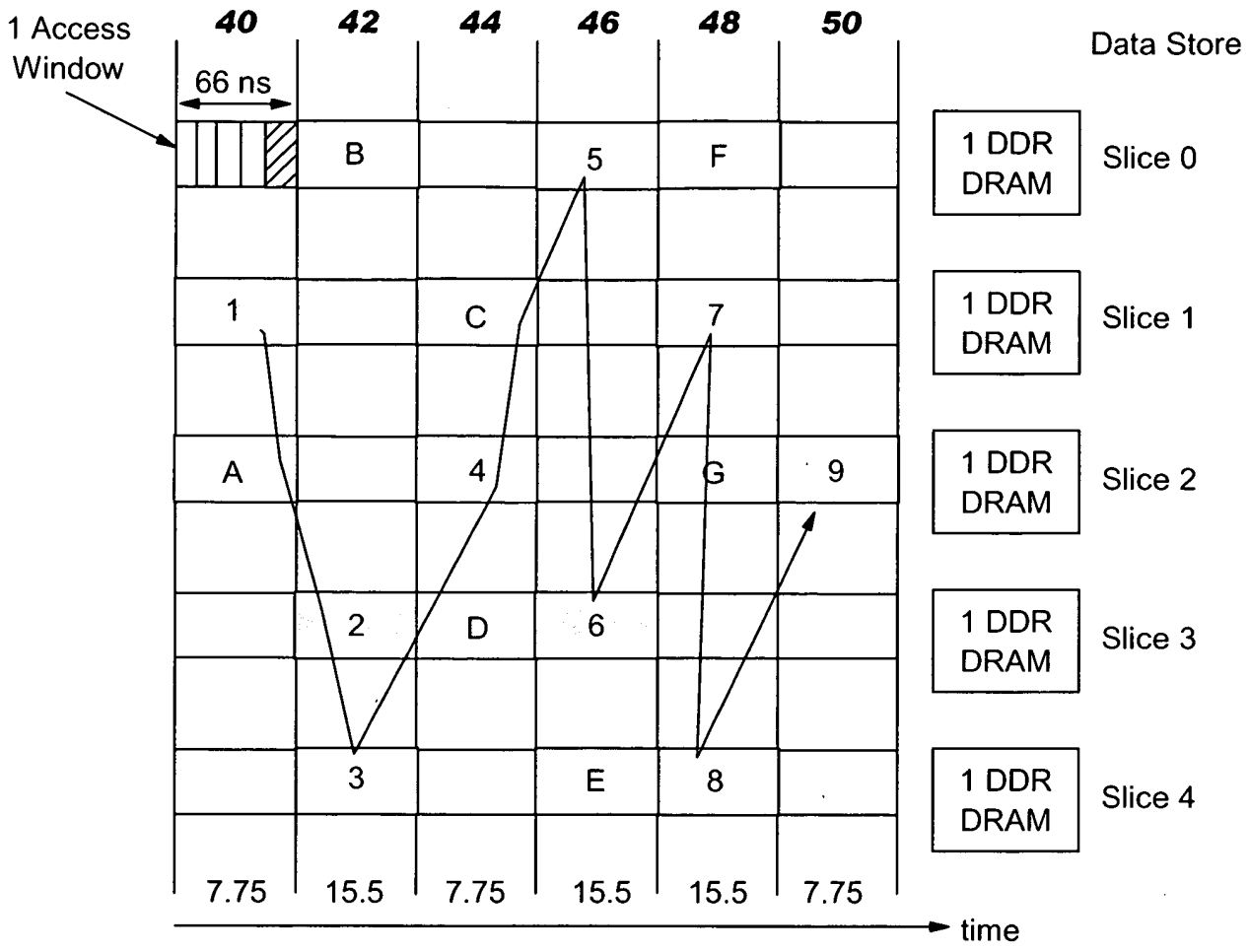

BUS IN
14 Gbps
Buffers are spread over 4 banks
DATA STORE
64x8 bits/(11x6 ns)= 7.75Gbps
SDM
2
3
EPC
RR
1
PMM
10Gbps
7.75Gbps
7.75Gbps
7.75Gbps
A
B
C
D
Slice_0
Slice_1
Slice_2
Slice_N
ARBITER
4 DDR DRAMs
x32 166 MHz

FIG. 6


1 Access Window
66 ns
40
42
44
46
48
50
Data Store
1 DDR DRAM
Slice 0
1 DDR DRAM
Slice 1
1 DDR DRAM
Slice 2
1 DDR DRAM
Slice 3
1 DDR DRAM
Slice 4
B
5
F
1
C
7
A
4
G
9
2
D
6
3
E
8
7.75
15.5
7.75
15.5
15.5
7.75
time